ATX7006

Measuring the reference current of a resistor ladder based D/A converter

This application note describes the possibility to make a graph of the reference load current as function of A/D converter code. The voltage over a sense resistor is measured using the ATX7006 WFD20 module in differential input mode.

Introduction

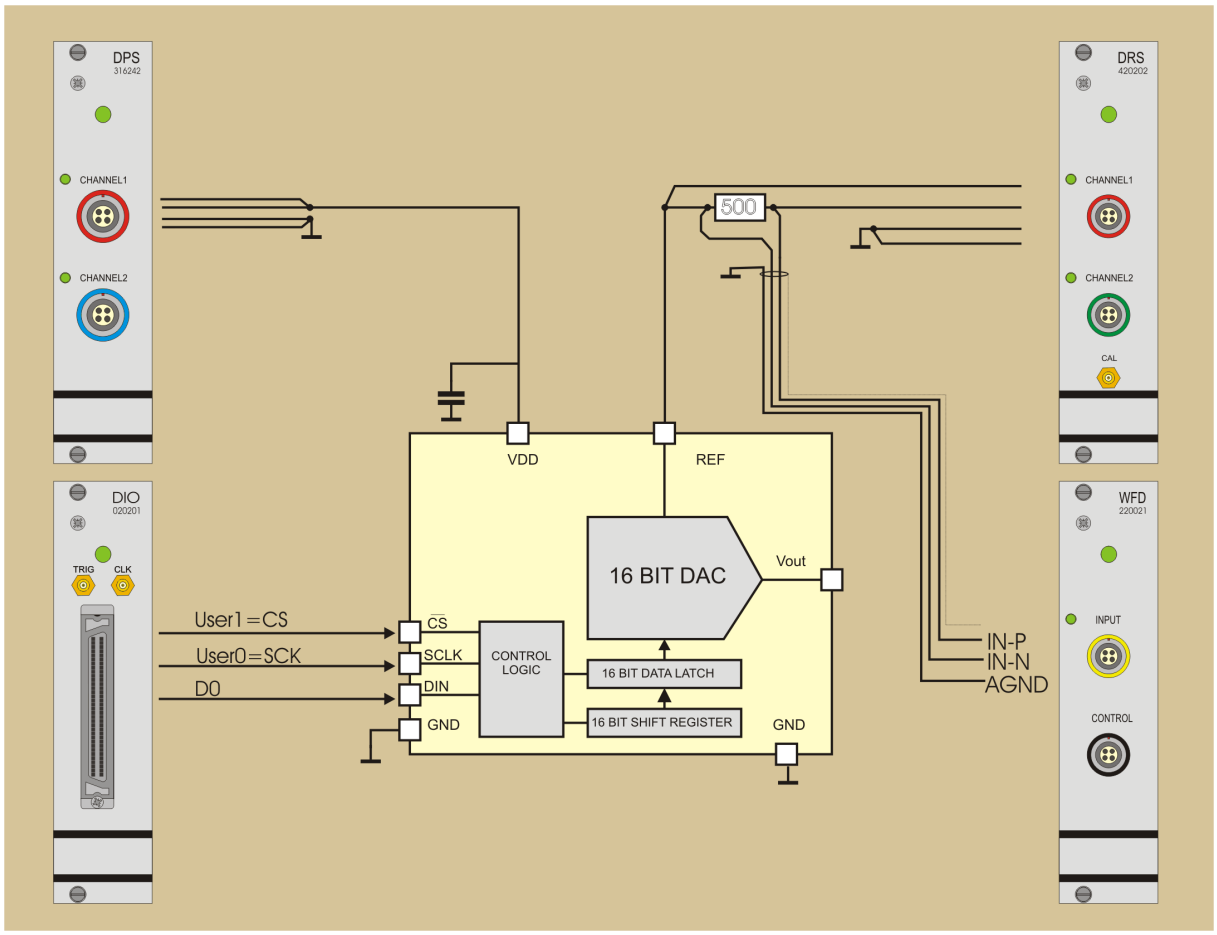
In some converter architectures, the reference current is dependent of the programmed DAC code. This code dependent reference input current, which can vary between the a few micro amps to approximately 2mA, is often neglected. In fact, a reference input may appear as a varying load to the reference source. When an external reference is applied, the voltage loss over the copper traces can significantly reduce the performance of a DAC. Since the voltage drop is not a fixed voltage, but varies with code, the use of a 4 wire sense circuit should then be considered. The ATX7006 reference DAC has a 4 wire connection option. The positive and negative sense lines should be connected close to the devices reference input pins or, in some cases, they can be connected to dedicated reference sense pins.

The converter

The converter, the LT2641-16, is a 16 bit serial D/A converter and has a voltage switching mode resistor ladder architecture. The four MSB's are decoded to drive 16 equally weighted segments. The remaining lower bits drive successively lower weighted sections. The specified impedance is specified as 14.8kOhms, this is the minimum impedance near halve scale of the device. At halve scale, the expected reference current is approximately 270uA at a reference voltage of 4 Volts. Although this reference current is rather low, it is very well possible to retrieve the exact reference current behavior.

Hardware setup

The figure shows a simplified schematic of the measurement setup.

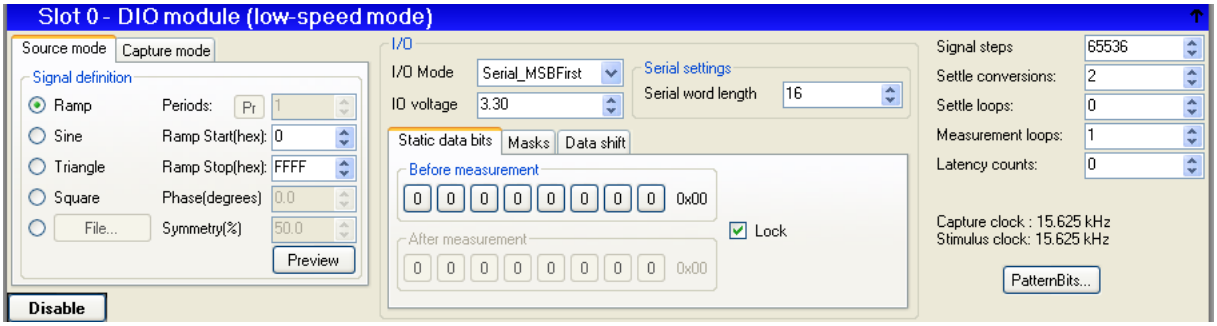


The DAC is controlled by the DIO. Two pattern bits from the pattern bit generator control the serial data transfer from the DIO to the DAC. The DPS module supplies a 5V supply voltage. The dual reference DAC is set to 4 volts and is connected to the REF input through a 500 ohms current sense resistor. The voltage drop across this resistor is compensated by the positive sense line, so a constant reference voltage on the device reference pin is assured. This voltage drop across the sense resistor represents the reference current and is differentially measured by the WFD module. At 200uA of reference current, a voltage drop of 100mV can be expected.

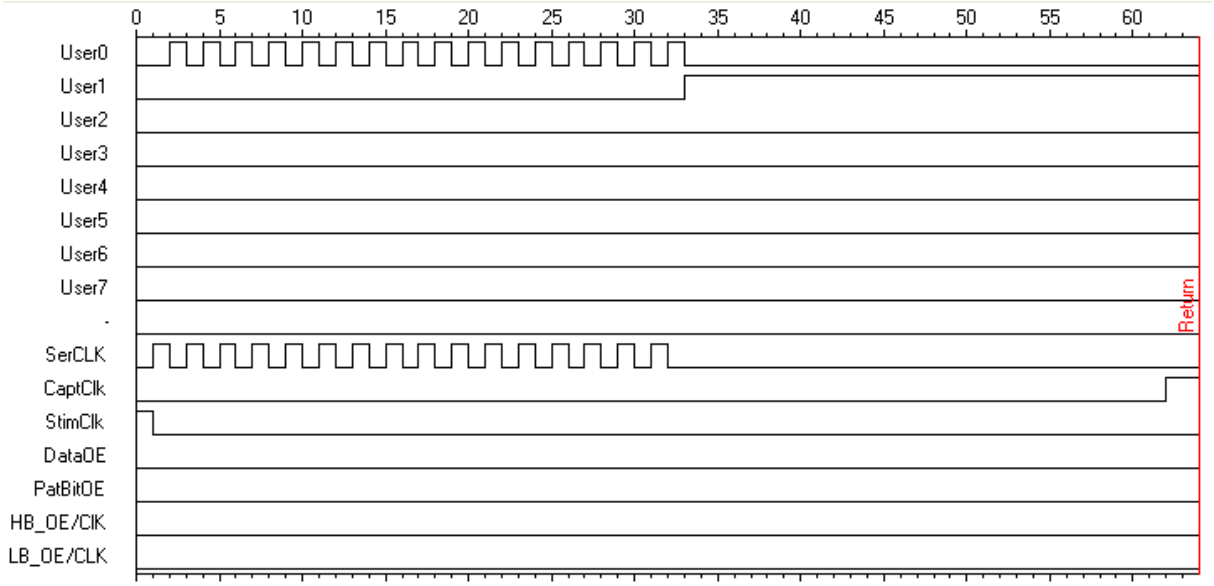
Setup of the DIO and the applied test signal

The DIO applies a digital ramp to the converter, from code 0 to code 0xFFFF. Two settle conversions are preceding the ramp. When the measurement is repeated, the DUT has the last converted code in its DAC register, which is the full scale code. So, at the start of the measurement, the DAC has to make a full scale swing. During the two settle conversions which are skipped in the analysis, the first ramp value is converted twice, so the output and WFD input gets the time to settle, before the actual measurement starts.

The IO mode is set to serial, MSB first, for the serial data transfer.



The DIO patternbit generator generates the two clocks needed for the serial data transfer: One internal clock, called SerClk for clocking the DIO shift register. The other one is “User 0” that is used as serial clock for the device under test.



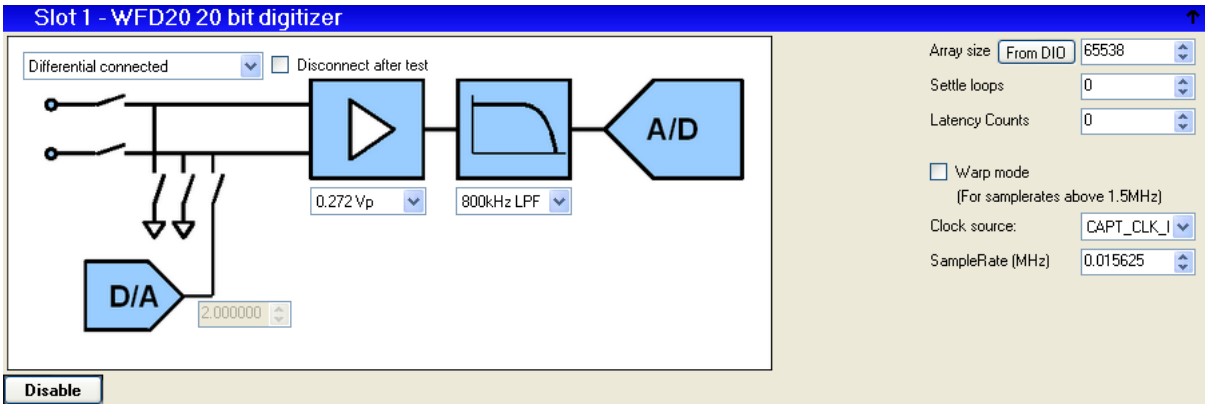
“User1” is connected to the chip select pin of the DUT. After shifting in the Data, the rising edge of CS clocks the serial data into the DAC register.

The stimulus clock (StimClk) clocks the stimulus generator and parallel loads the DIO serial shift register. StimClk is located just before the data shift. “CaptClk “is the sample clock for the AWG20 module. 34 patternbit steps after the CS rising edge, the output of the DAC has settled and the current in the reference is sampled.

WFD20 setup

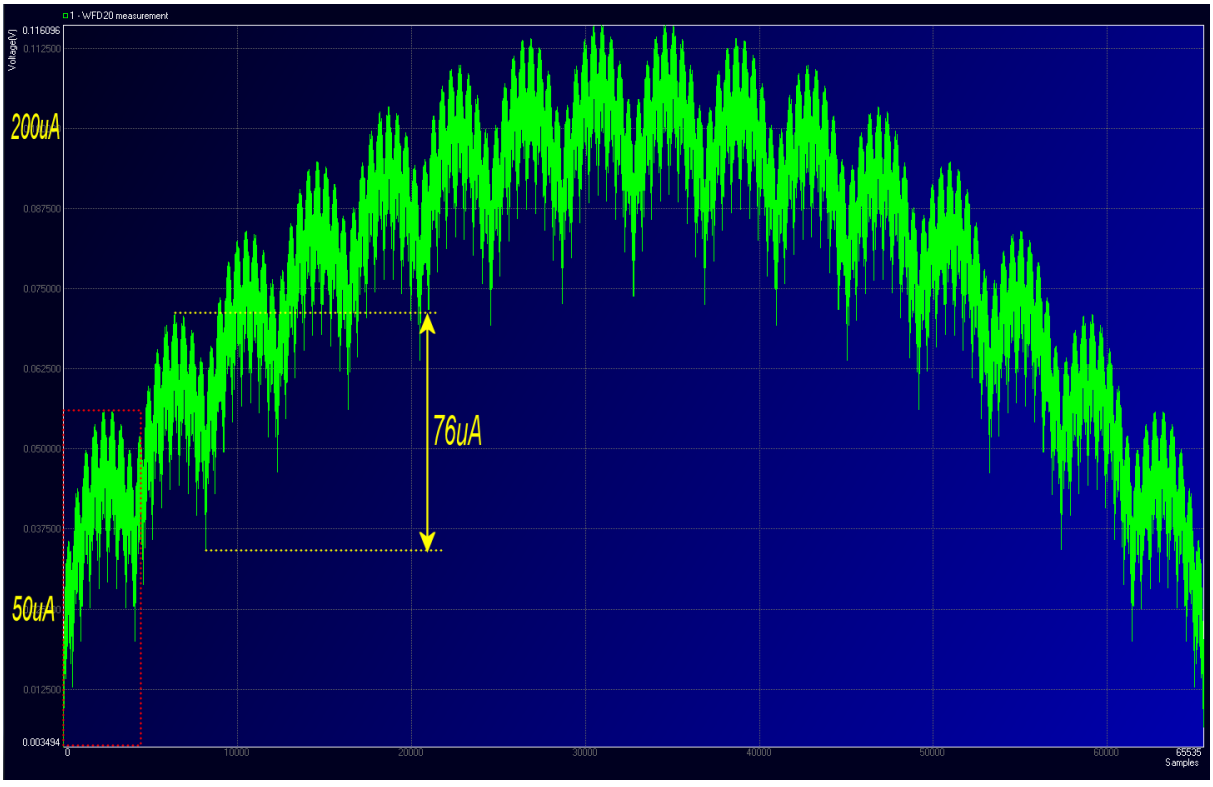
The WFD20 is connected differential over the sense resistor. The smallest input range of 0.272Vp is selected. To cancel out high frequent noise, the 800 kHz LPF is selected.

The capture array size is determined from the stimulus setting: 65536 steps+ 2 settle conversions. This setting is simply copied by clicking the “From DIO” button.



Analysis of the measurement results

In the ATView WaveAnalyzer tool, the results of the current measurement can be analyzed.

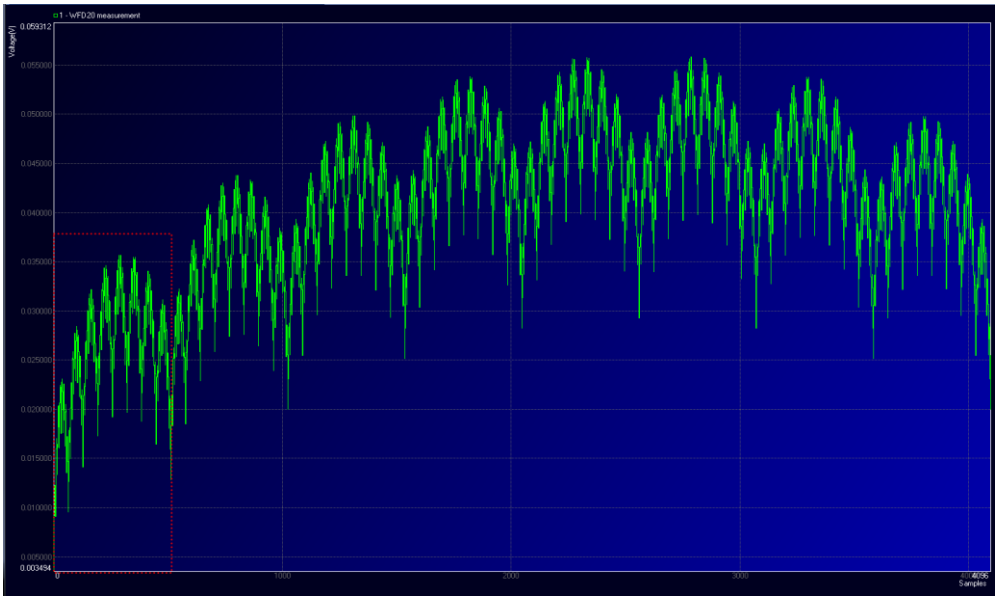


The figure shows a screenshot of the analyzer software, showing the measured voltage over the sense resistor for each converted code. On the horizontal axis are the ADC-codes.

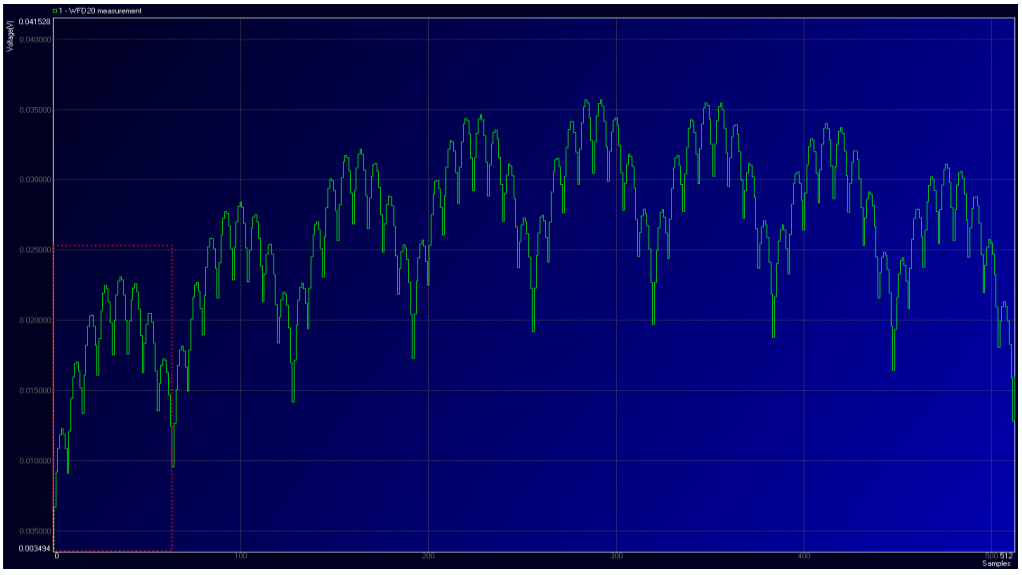
The vertical axis shows voltages that can be converted to currents, dividing by 500. The currents are manually added in the picture to clarify the actual currents measured.

The graph reveals the segmented architecture of the device. It is clear that the graph is subdivided in 16 sections. Each selected by the four most significant converter bits (bit 12, 13, 14 and 15).

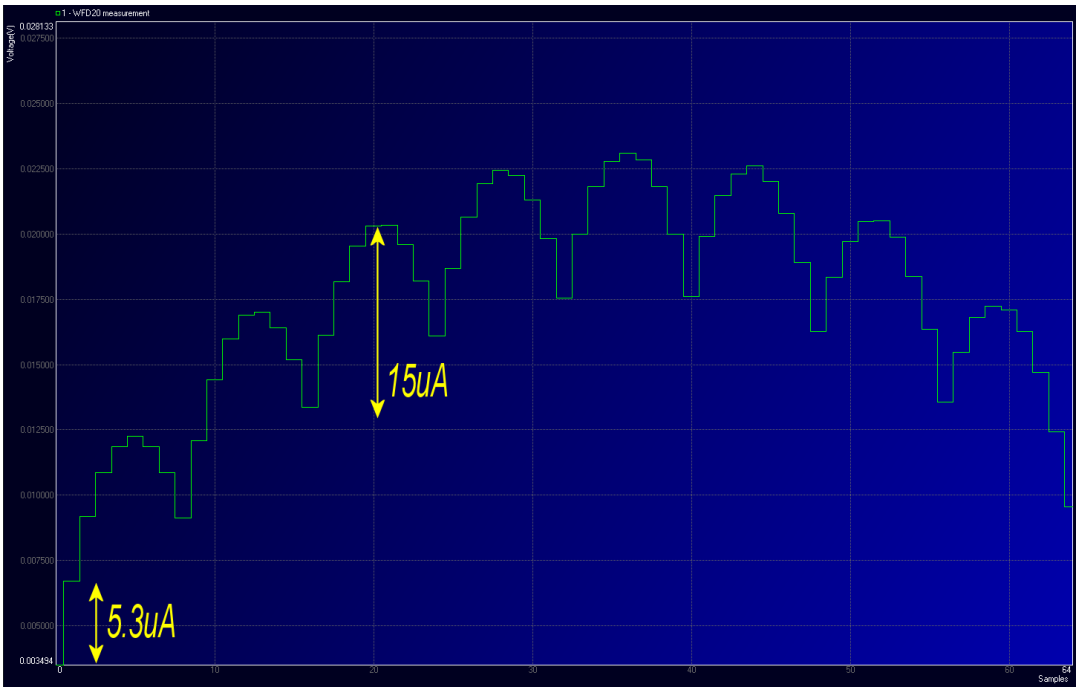
The figure below shows an enlargement of the first (dotted) section, the current flow for DAC code 0 to 4095.



Again, it is clear that this section, on its turn, is again divided in 8 subsections, selected by converter bit 9, 10 and 11. The first sub frame, indicated with the red dotted area, is in its turn enlarged.



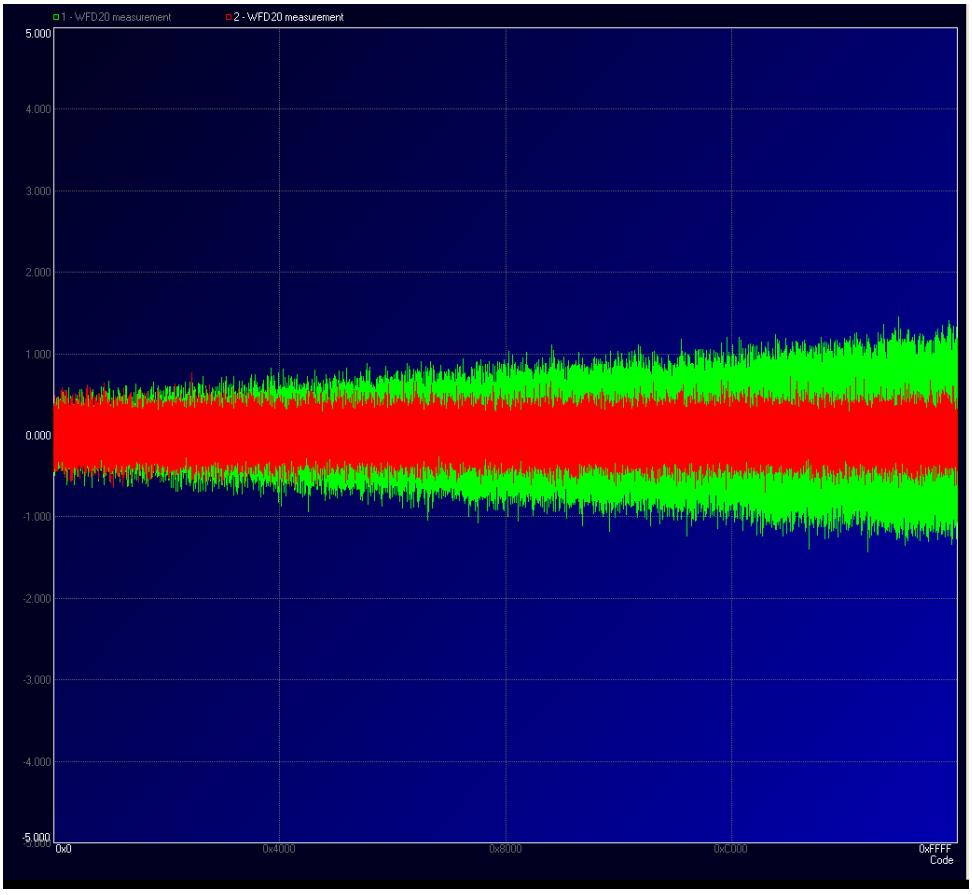
As expected, the enlarged subsection, visualizing the reference current for code 0...512, is divided into eight subsections that are selected by converter bit 6, 7 and 8. Finally, when we zoom in on the first sub section of this figure, we see the change in current when the lowest 6 significant bits are toggled.



The change in reference current for each code change is clearly unfolded in this graph, for input code 0 to 63.

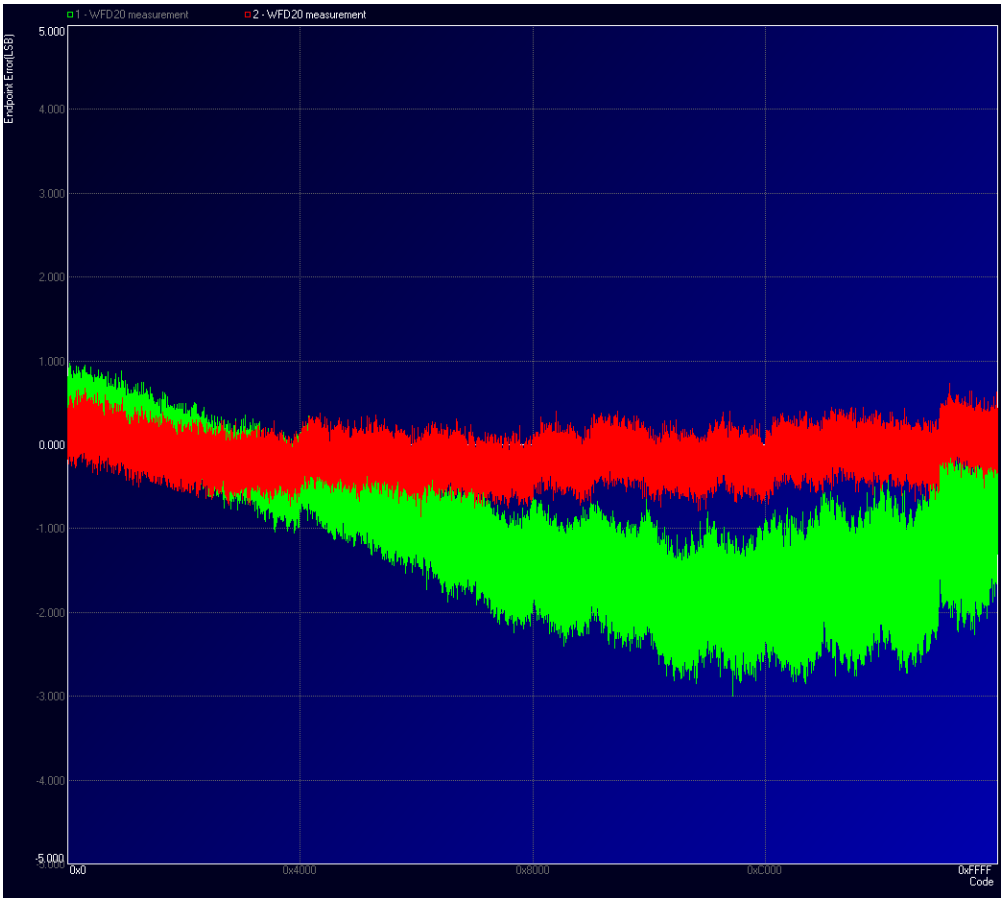
DNL degradation

In the graph below, the degradation of the converter DNL is shown. The red graph shows the DNL plot of the converter with a 4 wire reference connection.



The green plot shows the same converter but now with a 2 wire connection between the ATX reference and the converter. For this measurement, the 500 ohms sense resistor is removed in the test setup. The DNL degradation is also a result of reference GND noise that is normally compensated by the reference GND sense connection.

The endpoint plot shows the degradation in linearity due to the 2 wire reference connection.



Conclusion

Although the current in the reference is in the uA range, the reference current changes can easily be unveiled, by measuring the voltage drop over a sense resistor placed in the reference force line. Changes in reference current may result in degradation of the device performance when the reference source does not correct the voltage losses over cable and PCB copper traces.